

ABOV SEMICONDUCTOR
6 SEGMENT X 7 GRID LED DRIVER WITH KEYSKAN

MC2002

Data Sheet (Ver. 1.30)



Version 1.30

Published by
FAE Team

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REVISION HISTORY

VERSION 1.20 (2010. 05. 03) This Book

Modified the Key Scan data read sequence on page 17.

VERSION 1.20 (2010. 01. 07)

Modified the Operating Temperature on page 9.

VERSION 1.10 (2009. 04. 20)

Modified the Dout of Transmission (Data Read) FORMAT.

Modified the Key scan data read sequence.

VERSION 1.00 (2008. 12. 15)

The first Edition

DESCRIPTION

The MC2002 is specifically designed for LED and LED DISPLAY driver.

The MC2002 has max 9 segment output lines, max 7 grid output lines, one display memory, control circuit, 3 line serial data interface, and max 6 x 1 matrix key scan .

The more detail spec is listed below as Table 1.1.

Those functions are all incorporated into a single chip to build a highly reliable peripheral device for a single chip microcomputer.

It is very convenient to control for numeric display.

MC2002's pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantages.

FEATURES

- CMOS Technology
- Segment output line selection by command : 6 ~ 9
- Grid output line selection by command : 4~7
- Operation voltage : 2.7V ~ 5.5V
- Low Power Consumption
- 8-Step Dimming control by command
- Serial Interface for Clock, Data Input, Strobe Pins, Data output
- 20-pin TSSOP, 20-pin DIP Package

APPLICATION

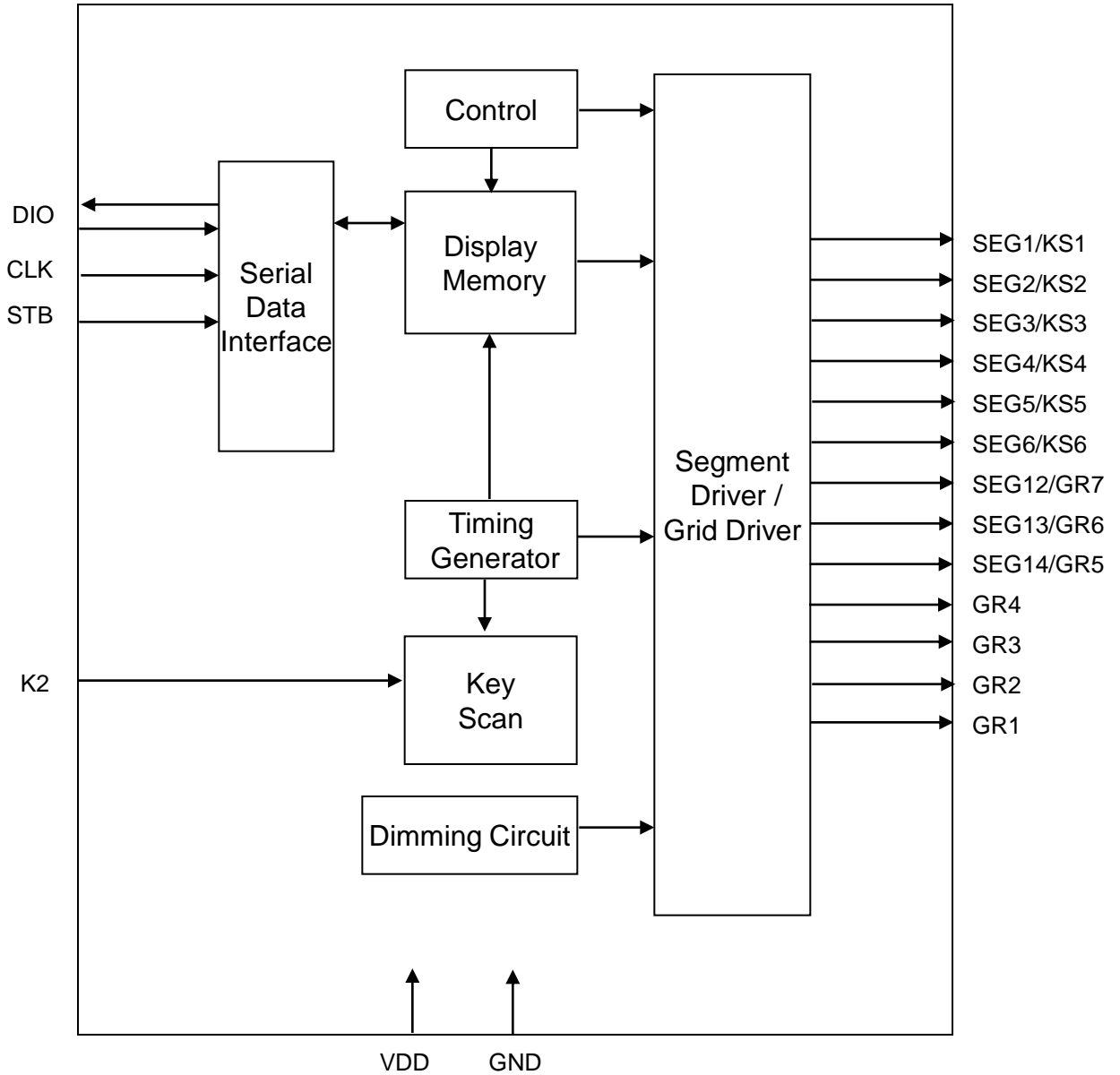
- Segment LED display : VCR, DVD, MWO

Device 명	Segment 수	Grid 수	Key Scanning	PKG TYPE
MC2002	6~9 Segment	4~7 Grid	6 X 1 Matrix	20pin, TSSOP, DIP

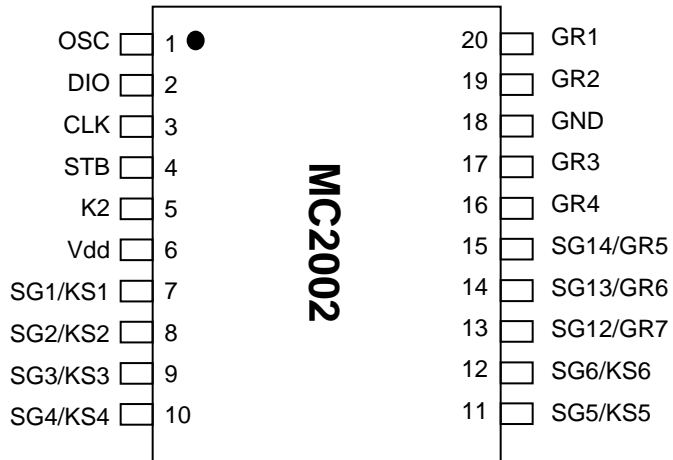
PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION	PIN No.
OSC	--	Oscillator Input pin. This pin is recommended open for operation.	1
DIO	I/O	Serial Data Input / Output Pin This pin outputs at CLK falling edge. This pin inputs serial data at the rising edge of CLK signal.	2
CLK	I	Serial clock input pin. Input data is trigger at rising edge. Output data is trigger at falling edge.	3
STB	I	When this pin is HIGH, CLK signal is ignored. The data input after the STB has fallen is processed as a command.	4
K2	I	Key scan input pins. This pins are operated with SEG1/KS1 to SEG10/KS10 pins. This pins have Pull down resistor internally.	5
VDD	-	Power Supply	6
SEG1/KS1 to SEG6/KS6	O	Segment output pins. (P-channel open drain) Also key scan source pins.	7~12
SEG12/GR7 to SEG14/GR5	O	Segment / Grid output pin.	13,14,15
GR4 to GR1	O	Grid output pin.	16,17 19,20
GND	-	Ground pin.	18

BLOCK DIAGRAM

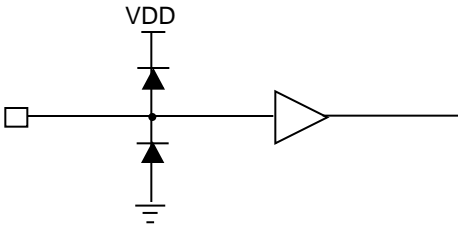


PIN CONFIGURATION

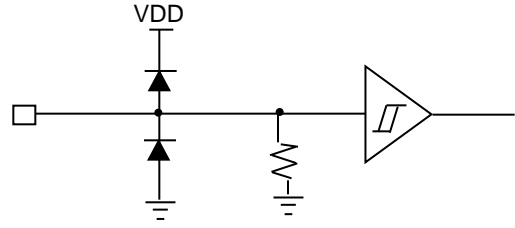


INPUT/OUTPUT PINS SCHEMATIC DIAGRAM

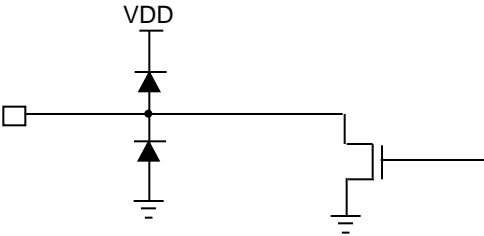
Input pins : CLK,STB



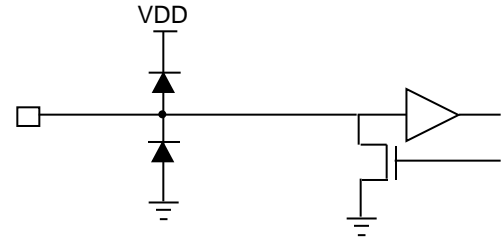
Input pins : K2



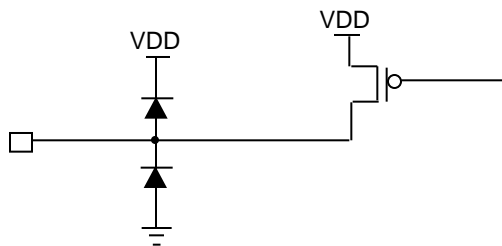
Output pins : GR1 to GR4



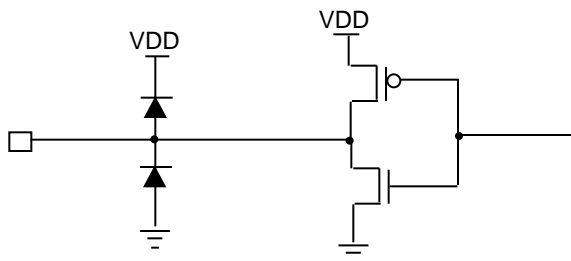
Input / Output pins : DIO



Output pins : SEG1/KS1 to SEG6/KS6



Output pin : SEG12/GR7 to SEG14/GR5



ABSOLUTE MAXIMUM RATINGS

(Ta=25°C, GND=0V)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	VDD	-0.5 to +7.0	V
Logic Input Voltage	VI	-0.5 to VDD+0.5	V
Driver Output Current/Pin	IOLGR	+250	mA
	IOHSG	-50	mA
Maximum Driver Output Current/Total	ITOTAL	400	mA

RECOMMENDED OPERATING RANGE

(Ta= -40 to +85°C, GND=0V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Logic Supply Voltage	VDD	2.7	5	5.5	V
Dynamic Current (see Note)	IDDdyn	-	-	5	mA
High-Level Input Voltage	VIH	0.6VDD	-	VDD	V
Low-Level Input Voltage	VIL	0	-	0.4 VDD	V

• Note : Test Condition : Set Display Control Commands = 80H (Display Turn OFF State)

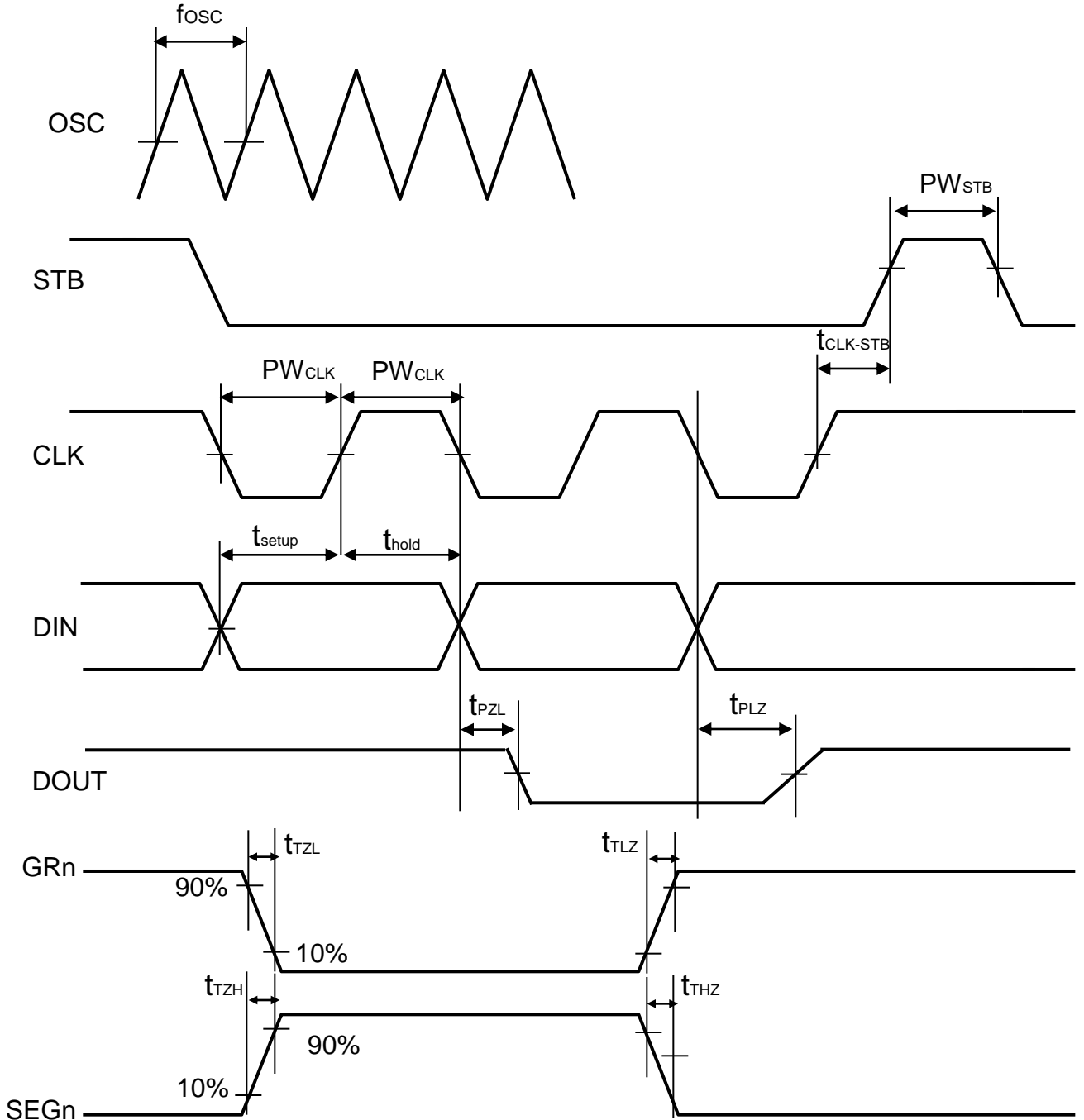
ELECTRICAL CHARACTERISTICS

(V_{DD}=5V, GND=0V, Ta=25°C)

PARAMETER	SYMBOL	Test Condition	Min.	TYP.	MAX.	UNIT
High-Level Output Current	IOHSG1	V _O = V _{DD} - 2V SEG1 to SEG11. SEG12/GR7 to SEG14/GR5	-20	-25	-40	mA
	IOHSG2	V _O = V _{DD} - 3V SEG1 to SEG11. SEG12/GR7 to SEG14/GR5	-25	-30	-50	mA
Low-Level Output Current	IOLGR	V _O = 0.3V GR1 TO GR4 SEG12/GR7 TO SEG14/GR5	100	140	-	mA
Low-Level Output Current	IOLDOU T	V _O = 0.4V DOUT	4	-	-	mA
Segment High-Level Output Current Tolerance	ITOLSG	V _O = V _{DD} - 3V SEG1 TO SEG11. SEG12/GR7 to SEG14/GR5	-	-	±5	%
High-Level Input Voltage	VIH	-	0.6VDD	-	VDD	V
Low-Level Input Voltage	VIL	-	0	-	0.4VDD	V
Oscillation Frequency	fOSC	-	350	500	650	kHz
K1 to K3 Pull Down Resistor	KSR	VDD=5V	40	-	100	kΩ

SWITCHING CHARACTERISTIC WAVEFORM

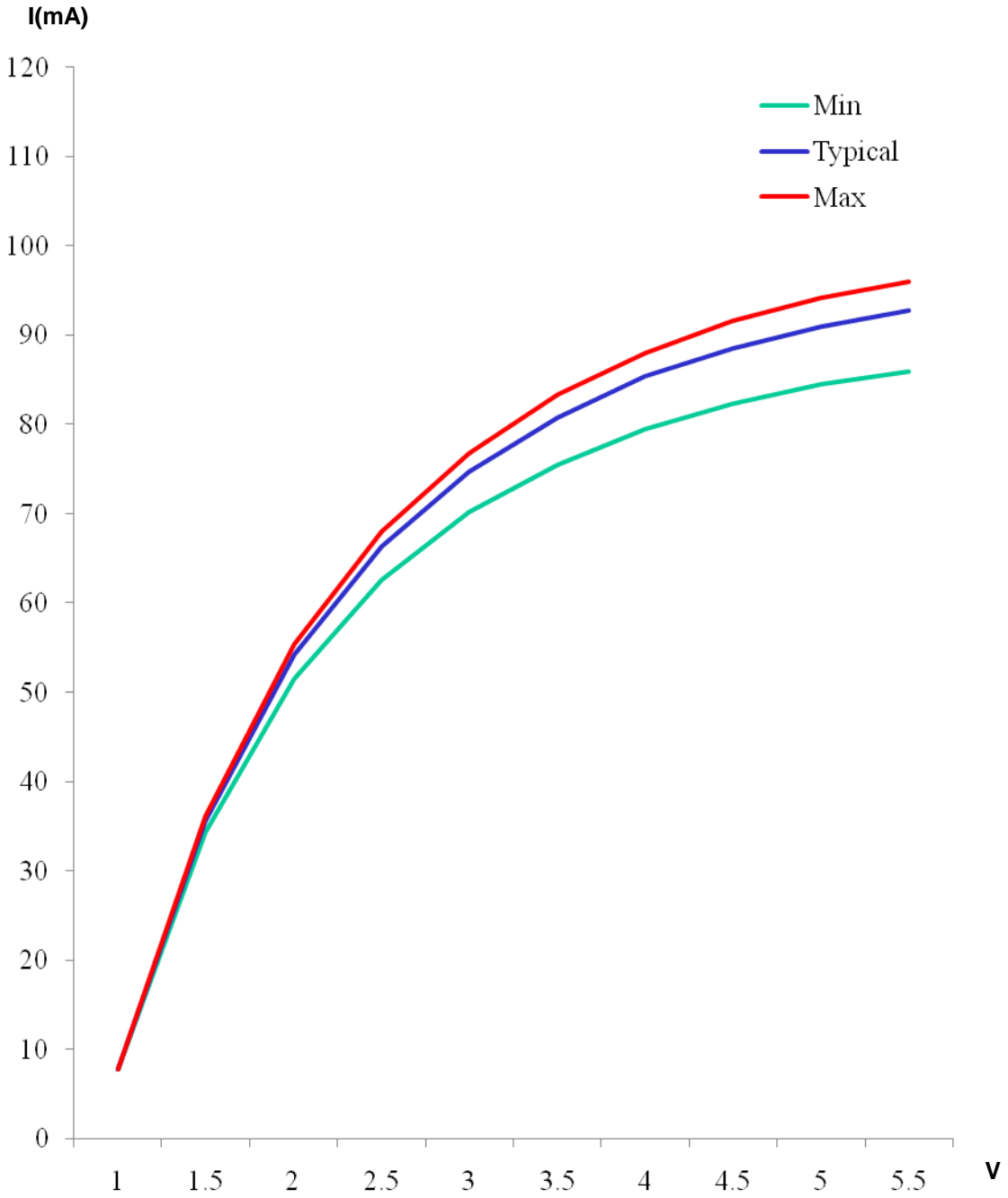
MC2002 Switching Characteristics Waveform is given below.



PW_{CLK} (Clock Pulse Width) $\geq 400ns$
 t_{setup} (Data Setup Time) $\geq 100ns$
 $t_{CLK-STB}$ (Clock - Strobe Time) $\geq 1\mu s$
 t_{TZH} (Rise Time) $\leq 1\mu s$
 $t_{TZL} < 1\mu s$

PW_{STB} (Strobe Pulse Width) $\geq 1\mu s$
 t_{hold} (Data Hold Time) $\geq 100ns$
 t_{THZ} (Fall Time) $\leq 10\mu s$
 f_{osc} = Oscillation Frequency
 $t_{TIZ} < 10\mu s$
 t_{PZL} (Propagation Delay Time) $\leq 100ns$
 t_{PLZ} (Propagation Delay Time) $\leq 300ns$

SEG PIN Resistance

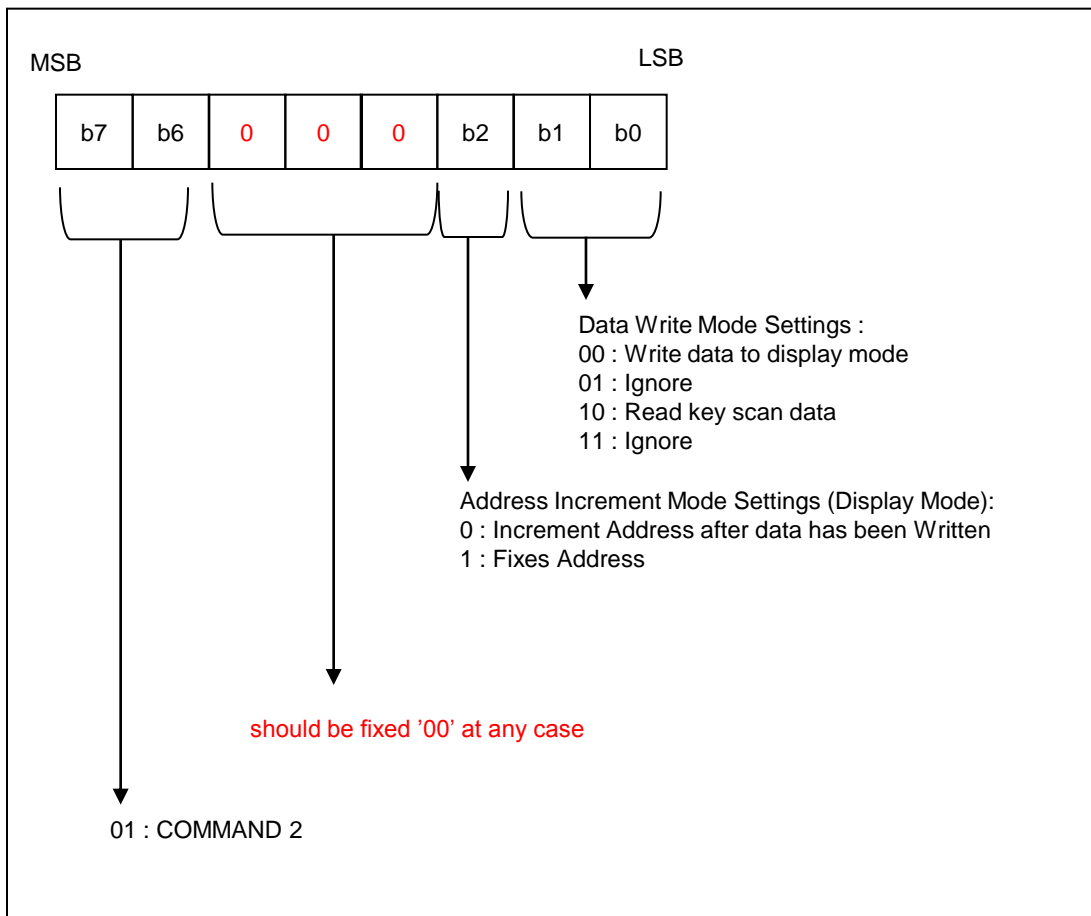


COMMAND 2 : DATA SETTING COMMAND

The data setting command consists of data write mode setting, address increment mode setting and mode setting. And the default of b3 to b0 are all "0" for power on.

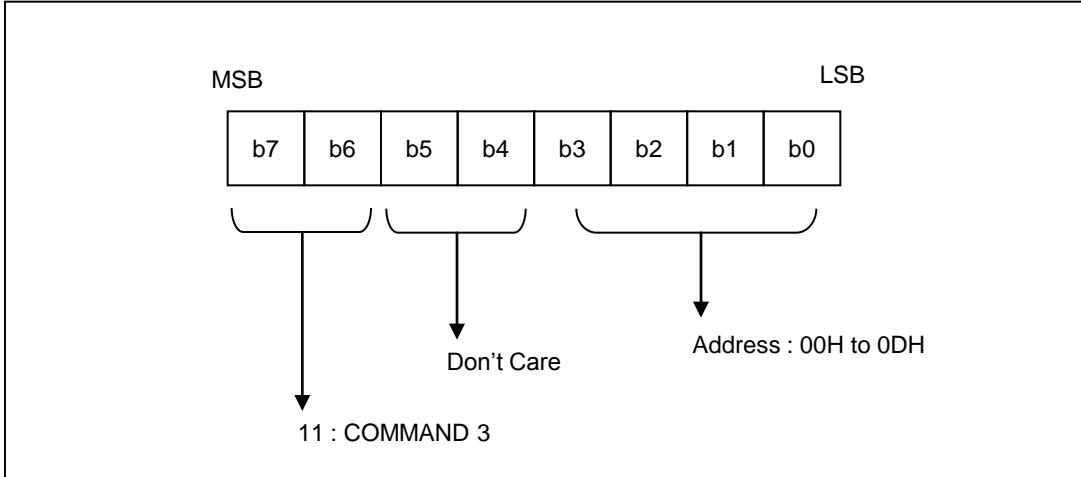
The Data write mode settings have 2bit (b1,b0) for writing data to display mode and read key scan data. Address increment mode setting has 1bit (b2) for selecting address Increment or fixed.

And 2bits(b5 ~ b3) should be fixed '000' at any case.
The command bits (b7,b6) are "0","1" for COMMAND2.



COMMAND 3 : ADDRESS SETTING COMMAND

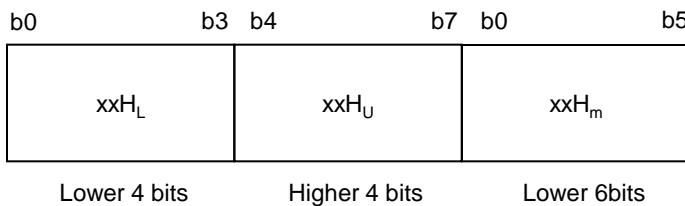
The display memory is addressed by Address Setting Command. The valid address range is "00H" to 0DH". If the address is set to 0EH to 0FH, the data is ignored until a valid address is set. When power is turned ON, the address is set at "00H".



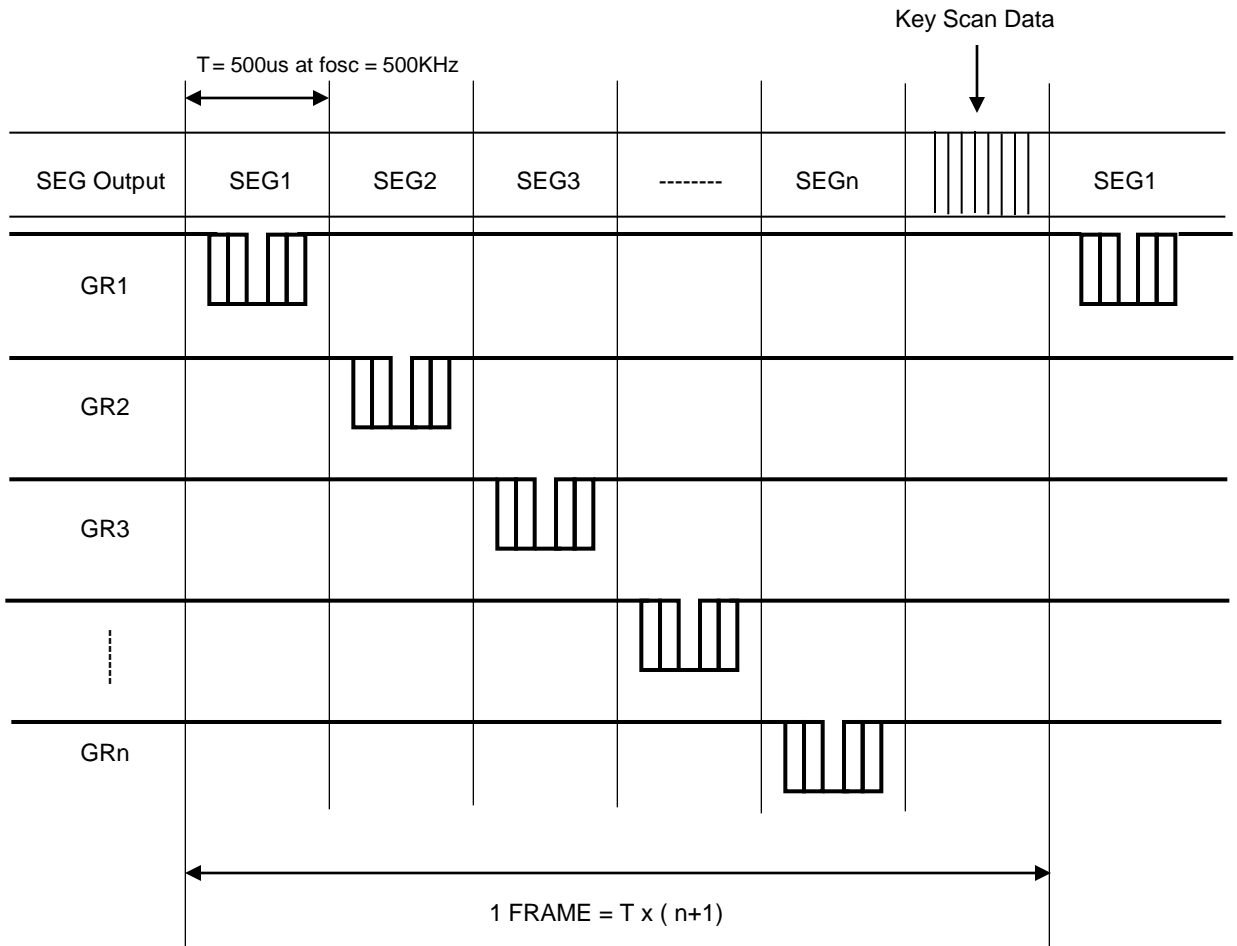
Display Mode and RAM Address

Data transmitted from an external device to MC2002 via the serial interface are stored in the Display RAM and are assigned addresses. The RAM Addresses of MC2002 are given below in 8 bit unit.

SEG1	SEG4	SEG5	SEG8	SEG9	SEG14	
00H _L		00H _U			01H _m	GR1
02H _L		02H _U			03H _m	GR2
04H _L		04H _U			05H _m	GR3
06H _L		06H _U			07H _m	GR4
08H _L		08H _U			09H _m	GR5
0AH _L		0AH _U			0BH _m	GR6
0CH _L		0CH _U			0DH _m	GR7



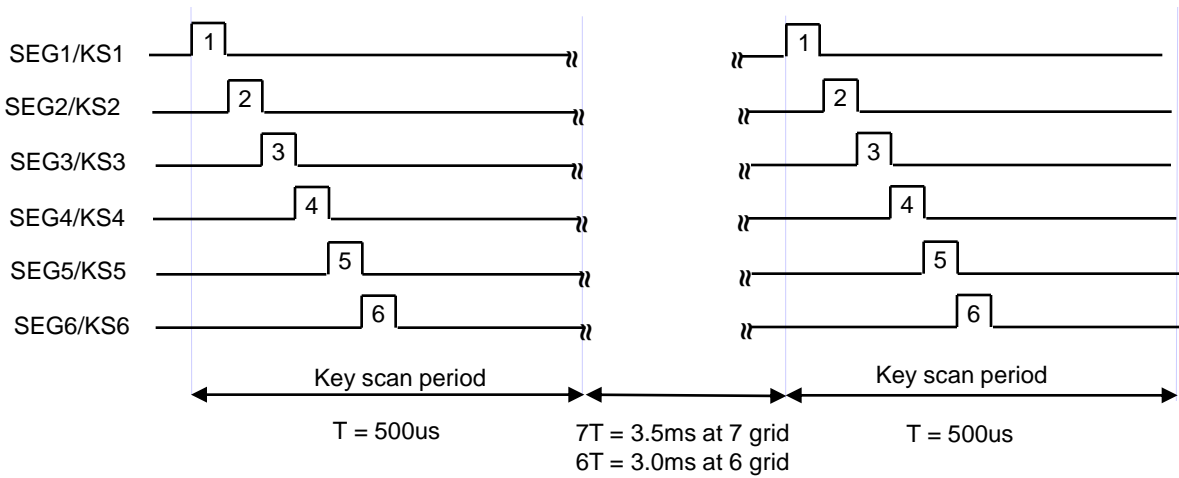
DISPLAY TIMING WAVEFORM



KEY SCAN

1) Key Scan Timing

The key scan period is 500us at oscillator=500Khz.



2) Key scan operation

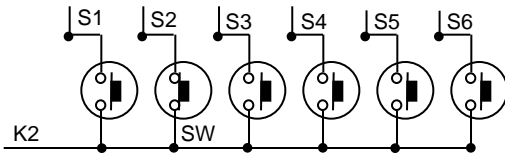
- The key scan is operated always.
- Multiple key presses are recognized by determining whether multiple key data bits are set.

3) Key scan data read sequence

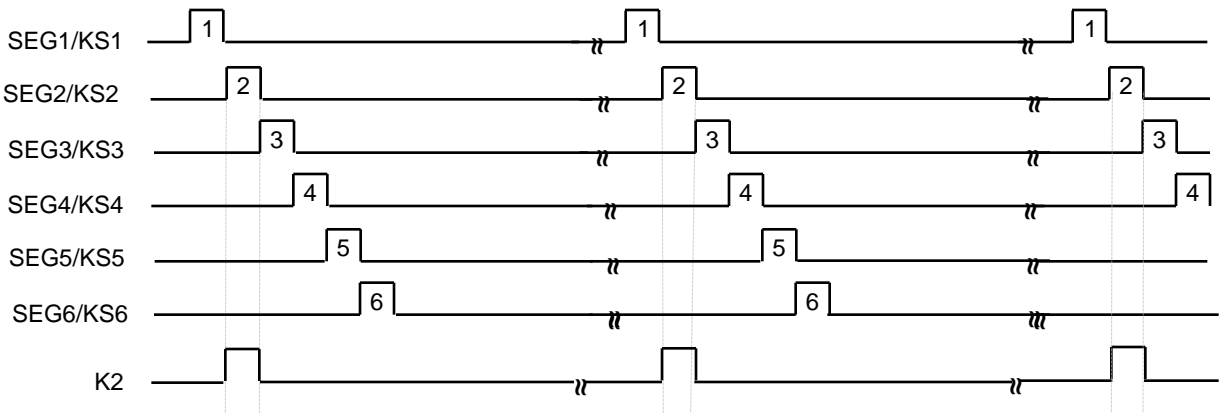
don't care	K2	don't care	don't care	K2	don't care			
X	SEG1/KS1	X	X	SEG2/KS2	X	0	1	1'st byte read
X	SEG3/KS3	X	X	SEG4/KS4	X	0	1	2'nd byte read
X	SEG5/KS5	X	X	SEG6/KS6	X	0	1	3'rd byte read
X	X	X	X	X	X	0	1	4'th byte read
X	X	X	X	X	X	0	1	5'th byte read
X	X	X	X	X	X	0	1	6'th byte read
b0	b1	b2	b3	b4	b5	b6	b7	

Key press = "1", Key no press = "0" read.

4) Key Scan Example



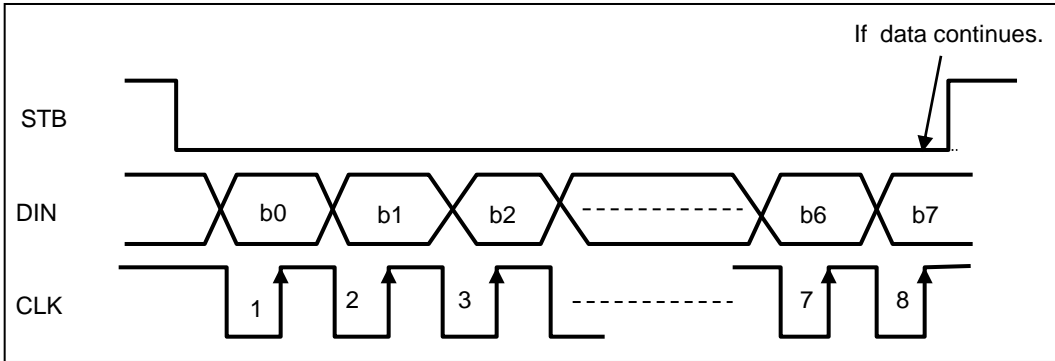
If SW switch is pressed, the K2 of key input pin is high by S2 at key scan timing.
So the K2 pin input is high.



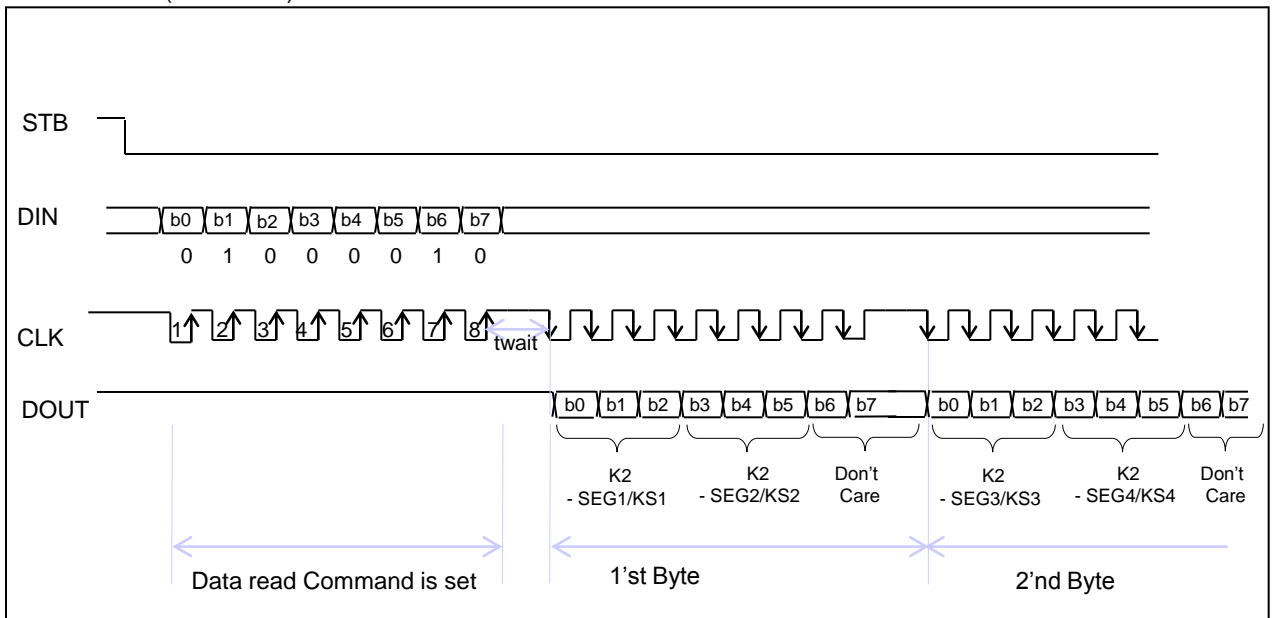
SERIAL COMMUNICATION FORMAT

The following diagram shows the MC2002 serial communication format.

RECEPTION (Data/Command Write)



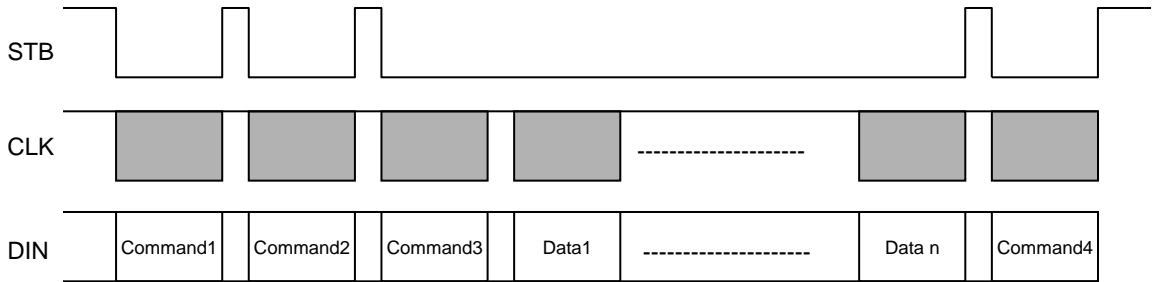
Transmission (Data Read)



Twait (waiting Time) $\geq 1\mu s$

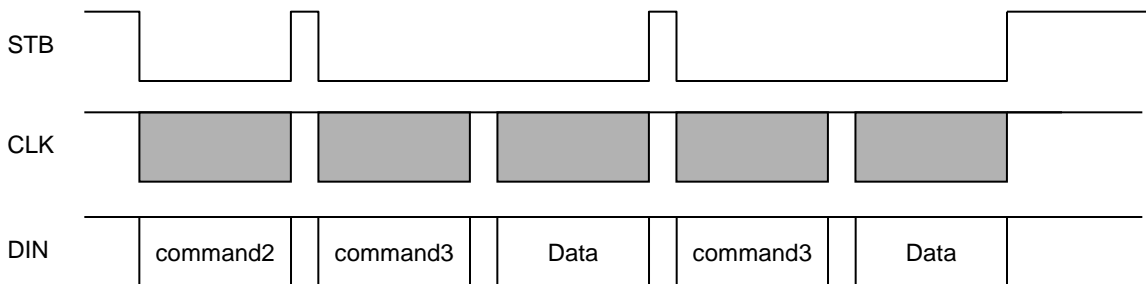
SERIAL COMMUNICATION EXAMPLES

Serial communication timing diagram for initialization setting.



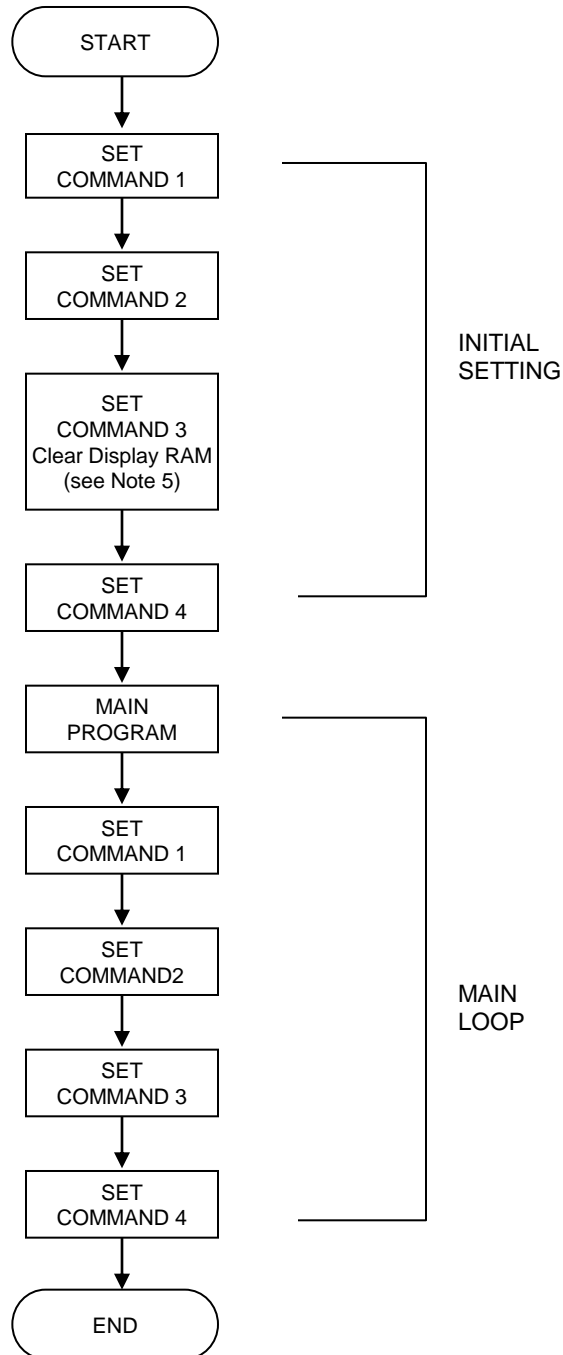
Where : Command 1 : Display Mode Setting
 Command 2 : Data Setting Command
 Command 3 : Address Setting Command
 Data 1 to n : Transfer Display Data (14 Bytes max.)
 Command 4 : Display Control Command

Memory updating timing diagram.



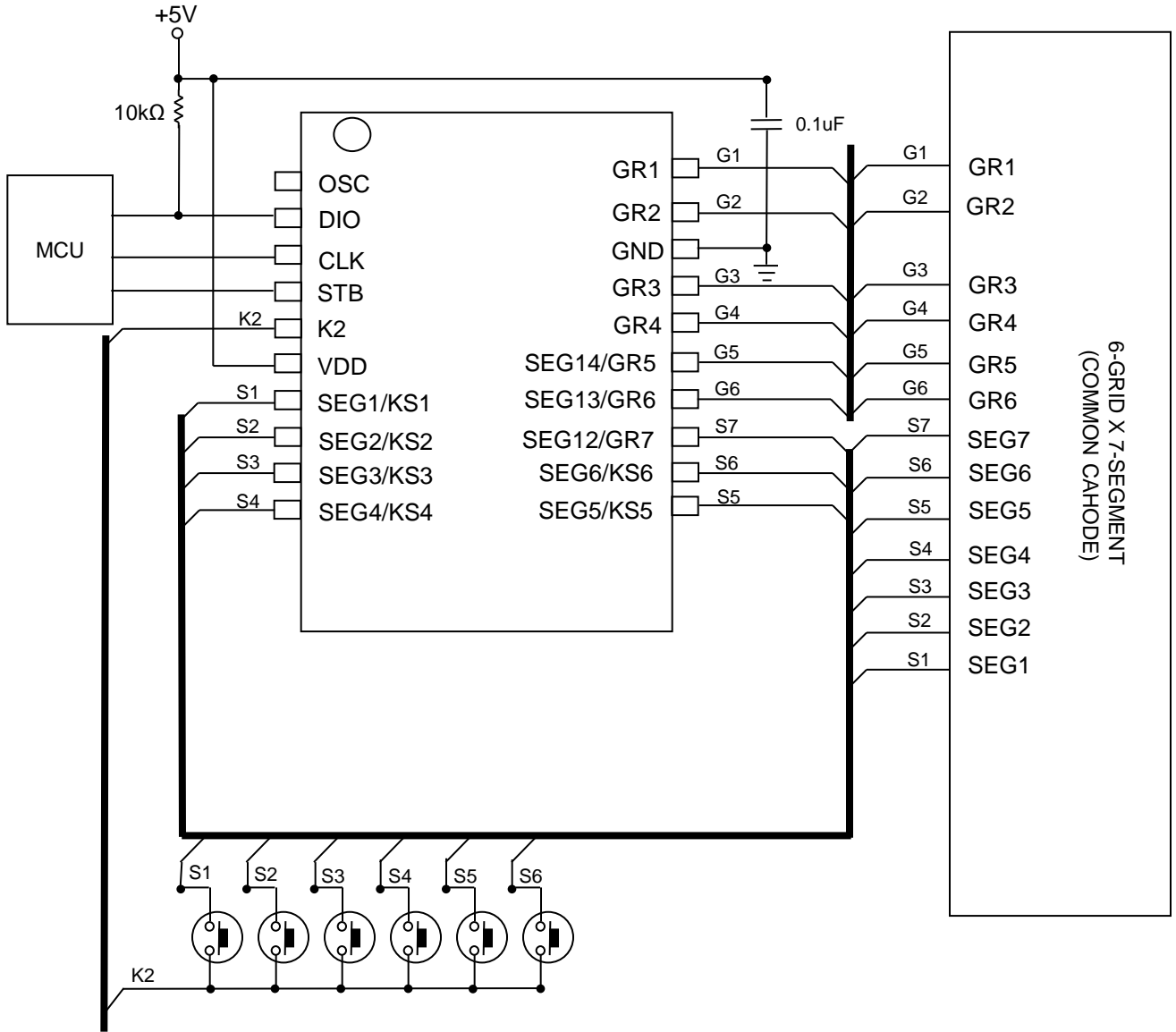
Where : Command 2 -- Data Setting Command
 Command 3 -- Address Setting Command
 Data -- Display Data

RECOMMENDED SOFTWARE PROGRAMMING FLOW CHART

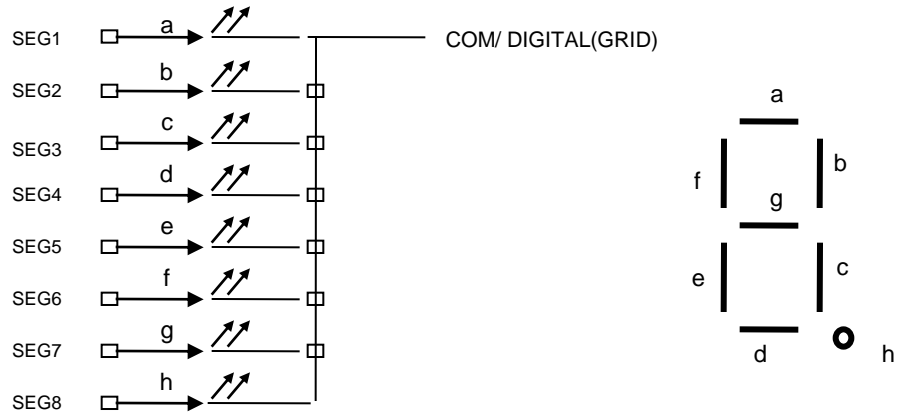


- **Note** : 1. Command 1 : Display Mode Setting
- 2. Command 2 : Data Setting Commands
- 3. Command 3 : Address Setting Commands
- 4. Command 4 : Display Control Commands
- 5. When IC power is applied for the first time, the contents of the Display RAM are not defined : thus, it is strongly suggested that the contents of the Display RAM must be cleared during the initial setting.

TYPICAL APPLICATION CIRCUIT



LED PANEL FOR CATHODE TYPE



PACKAGE INFORMATION

TSSOP 20

